

GenGNN: A Generic FPGA Framework for Graph Neural Network Acceleration

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Abstract

Graph neural networks (GNNs) have recently exploded in popularity thanks to their broad applicability to ubiquitous graph-related problems such as quantum chemistry, drug discovery, and high energy physics. However, meeting demand for novel GNN models and fast inference simultaneously is challenging because of the gap between the difficulty in developing efficient FPGA accelerators and the rapid pace of creation of new GNN models. Prior art focuses on the acceleration of specific classes of GNNs but lacks the generality to work across existing models or to extend to new and emerging GNN models. In this work, we propose a generic GNN acceleration framework using High-Level Synthesis (HLS), named **GenGNN**, with two-fold goals. First, we aim to deliver ultra-fast GNN inference without any graph pre-processing for real-time requirements. Second, we aim to support a diverse set of GNN models with the extensibility to flexibly adapt to new models. The framework features an optimized message-passing structure applicable to all models, combined with a rich library of model-specific components. We verify our implementation on-board on the Xilinx Alveo U50 FPGA and observe a speed-up of up to 25× against CPU (6226R) baseline and 13× against GPU (A6000) baseline. Our HLS code will be open-source on GitHub upon acceptance.¹

1 Introduction

Graph neural networks (GNNs) have become a powerful tool for applying deep learning to solve tasks infilling graph structures. Learning tasks for graphs can be applied at node-level (e.g., presence of protein [1]), edge-level (e.g., drug-drug interactions [2]), and graph-level (e.g., molecular property prediction [3]). Representative applications of GNNs include analysis of social networks and citation networks, recommendation systems, traffic forecasting, LIDAR point cloud segmentation for autonomous driving, high energy particle physics, and molecular representations [4].

Targeting various applications, there is a huge demand for GNN inference acceleration with diverse **requirements**. For instance, point cloud segmentation and detection for autonomous driving [5] and high energy particle physics [6]

require *real-time processing*; in a particular example, the collision data from particle collider are collected every 25ns and thus must be processed using GNNs within nanoseconds with raw input graphs [7, 8]. For social network applications, the size of the graphs to be processed is usually extremely huge and the computation time and memory cost are significant; therefore, such applications are in demand for GNN accelerators for *large-scale* graphs. Consequently, hardware acceleration is critical to apply GNNs to these applications and address real-time or large-scale computation.

The **challenges** and the **limitations** of existing accelerators, however, are significant. First, GNN computation is both communication-intensive and computation-intensive, as also noted by previous literature [9–11], involving massive irregular memory access for message passing and heavy computation for embedding transformation. Second, novel GNN models are rapidly emerging while the accelerator innovation is lagging behind. For instance, most state-of-the-art GNN accelerators are tailored for graph convolutional networks (GCNs) [9, 12, 13], which can be conveniently expressed as sparse matrix multiplications (SpMM). However, the majority of GNNs are not suitable for SpMM because of complicated operations such as edge embedding, attention, mixed neighborhood aggregation, etc. Therefore, *generic, extensible, and flexible acceleration frameworks* are required to rapidly adapt to evolving GNN models. Third, some accelerators adopt graph preprocessing to employ data locality [9, 14–17], while some apply graph partitioning relying on the property of a fixed input graph (e.g., by analyzing the adjacency matrix sparsity [13]). Such preprocessing or graph-specific techniques *are not feasible* for real-time applications with millions of input graphs with varied structures.

Motivated by the emerging requirements and existing limitations, we propose a generic and flexible framework on FPGA for GNN acceleration, named **GenGNN**, which supports a wide range of prevailing GNNs and is extensible for new models. Highlighting the features of **GenGNN** in Table 1, we summarize our contributions as follows:

- GenGNN is the *first generic* GNN acceleration framework that can process a large variety of GNNs with on-board implementation. Table 2 summarizes the currently supported GNN models; each is a representative of a large GNN family. The framework is also dataset and graph

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¹<https://github.com/sharc-lab/GenGNN>

Feature	SOTA FPGA Accelerators	Ours (GenGNN)
Generic	✗: GCN only [9, 13]; ✗: heavily rely on the property of a specific graph (e.g., sparsity) [13]	✓: Support a wide types of GNNs; ✓: GNN, dataset and graph structure agnostic
Real-time	✗: Requires heavy graph preprocessing [9] or partitioning on CPU [13]	✓: Zero preprocessing; directly takes in raw graphs and processes on FPGA
Open-source	✗: Not yet	✓: Open-source with executables upon publication

Table 1. Comparisons between our **GenGNN** framework and existing FPGA-based accelerators; our main advantages are *generic*, *real-time*, and *open-source*.

Model	SOTA	Ours	Representativeness
GCN [18]	✓ F* [9]	✓	GNN family that can be represented as sparse matrix-matrix multiplications (SpMM)
GIN [19]	⊙ A [†] [17]	✓	GNN family with edge embedding and transformation where SpMM <i>does not</i> apply
GAT [20]	⊙ A [†] [11]	✓	GNN family with self-attention and possibly edge embeddings
PNA [21]	✗	✓	A popular GNN family arbitrarily using multiple aggregation methods
DGN [22]	✗	✓	A state-of-the-art GNN with a directional flow at each node and guided aggregation
VN [23]	✗	✓	A widely used GNN technique with a virtual node connecting to all other nodes

F*: FPGA implementation; A[†]: ASIC implementation; GCN: graph convolutional network; GIN: graph isomorphism network; GAT: graph attention network; PNA: principal neighbourhood aggregation; DGN: directional graph network; VN: GNN with virtual node

Table 2. Currently prototyped representative GNNs by our framework **GenGNN** with easy extension to more types.

structure agnostic, i.e., does not rely on the analysis for a specific input graph.

- GenGNN is also the first to target *real-time* applications with *zero preprocessing* and partitioning, where the graphs are streamed in consecutively.
- GenGNN is developed using High-Level Synthesis (HLS) for ease-of-use with modularized processing elements (PEs) for GNN components for extensibility. We will open-source the framework with an on-board executable for each GNN model upon acceptance.
- GenGNN is composed of a novel and highly optimized *message passing* architecture, which accommodates the majority of state-of-the-art GNNs. It also includes a rich library of model-specific components, where new GNN components can be developed and plugged in seamlessly.
- We extensively conduct experiments on two popular datasets with more than 45k graphs and three widely used large graphs. Our measurements are *on-board* execution with guaranteed *end-to-end correctness* by cross-checking with PyTorch implementation. **GenGNN** on Xilinx Alveo U50 FPGA achieves a speed-up of up to 25× against CPU (6226R) baseline and 13× against GPU (A6000) baseline.

2 Related Work

GNN acceleration is attracting intensive attention in the research community. Recent works are summarized by a survey [24], including both ASIC and FPGA accelerators.

The majority of the accelerators are targeting ASICs via simulation. For instance, HyGCN [17] is one of the earliest which introduces a hybrid architecture for GCN acceleration. EnGN [25] uses PEs connected in a ring and performs aggregations using a technique called Ring-Edge Reduce, while GRIP [26] uses the GReTA abstraction [27] to enable acceleration of any GNN variant. AWB-GCN [12] aims to combat workload imbalance in graph processing, while GCNAX [28] addresses the shortcomings of resource underutilization and excessive data movement using a flexible dataflow.

On the other hand, FPGA-based accelerators primarily focus on GCN acceleration. Zhang *et al.* [9] combine software preprocessing with hardware utilizing both node-level and feature-level parallelism, while BoostGCN [13] specifically optimizes GCN via sparsity analysis and graph partitioning. Auten *et al.* [11] propose an architecture that uses general-purpose CPUs connected by a network-on-chip to accelerate various GNNs. Rubik [16] and GraphACT [29] aim to accelerate GCN training using ASIC and FPGA, respectively.

Limitations. The computation pattern of GCN can be abstracted as a series of sparse and dense matrix multiplications so that most accelerators focus on optimizing the SpMM kernels. However, advanced GNNs such as PNA, GAT, and GIN require more complex compute patterns than SpMM. These models use aggregators besides sum aggregation and require materialization of neighboring nodes to compute edge embeddings, which must be done explicitly on a per-node basis. In addition, many of these accelerators also adopt off-chip preprocessing such as graph partitioning, which in real-time applications is not possible.

In the following, we introduce the overall architecture of **GenGNN** in Section 3, and discuss the rich model-specific libraries in Section 4. Performance is presented in Section 5.

3 Generic Architecture of GenGNN

3.1 GenGNN Framework Features

GenGNN Features. Our goal is to provide a generic and real-time FPGA acceleration framework for a wide range of GNNs, with great flexibility to support emerging GNNs with minimum modification in a plug-in manner. Table 1 summarizes our key features compared with state-of-the-art FPGA accelerators. **① Generic.** While most existing FPGA works are limited to GCN by formulating GNN computation as SpMM, **GenGNN** supports a wide variety of GNN types by constructing a *message passing* architecture to which most GNNs belong. It can also accept arbitrary dataset and graph structures. **② Real-time.** In practical applications such as point clouds in autonomous driving and particle graphs in

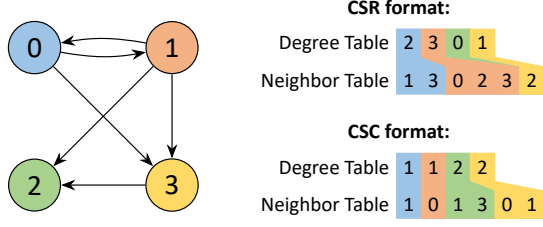


Figure 1. An example graph and the equivalent representations of its adjacency matrix in CSR and CSC formats.

high energy physics, the graphs are constructed and must be processed in real-time, leaving no time for preprocessing, partitioning, or adjacency matrix analysis. Different from accelerators that rely on a preprocessing/partitioning optimization, **GenGNN** directly processes raw graphs consecutively, targeting real-time inference for a large number of graphs. **3 Open-source.** We will open-source our framework written in HLS to encourage more GNNs to be built on top of **GenGNN** to promote a GNN acceleration ecosystem.

Supported GNNs. Table 2 summarizes currently supported GNNs, each being representative of a family of GNNs. Graph convolutional network (GCN) [18] represents the ones can be formulated as sparse matrix-matrix multiplications (SpMM); simplified GCN [30] also falls into this category. Graph isomorphism network (GIN) [19] represents advanced GNNs with higher representation power, including edge embeddings and transformations where SpMM *does not* apply; GraphSage [31] falls into this category. Principal neighborhood aggregation (PNA) [21] represents a popular GNN family that uses multiple arbitrary aggregation methods simultaneously. Graph attention network (GAT) [20] represents a GNN family with multi-head self-attention and possibly with edge embeddings. Directional graph network (DGN) [22] is a state-of-the-art GNN with directional flow at nodes with guided aggregation. GNN with virtual node (VN) [23] is a widely used GNN technique using virtual nodes connected to all other nodes. In addition, GenGNN supports both node-level and graph-level tasks (easily extended to edge-level tasks), and is scalable to both small and large graphs.

3.2 Graph Data Representation

The input graphs for GNNs typically have sparse adjacency matrices, which can be stored in different formats.

COO. In **CO**ordinate format, edges are stored in an arbitrarily-ordered list, where each list entry consists of the source node, the destination node, and the data associated with the edge. COO format is convenient for graph producers and is usually the raw graph format in real-time applications, but can be less performant for graph consumers.

CSR. In **C**ompressed **S**parse **R**ow format, adjacency information is stored in three arrays. The first is the degree table,

Notation	Description
$\mathcal{G} = (A, X, E)$	The input graph for the GNN
$A \in \mathbb{R}^{N \times N}$	Adjacency matrix of $\mathcal{G}$ (N : number of nodes)
$x_i^l \in X \in \mathbb{R}^{N \times F}$	Node embedding of node i at layer l
$e_{i,j}^l \in E \in \mathbb{R}^{M \times D}$	Edge embedding of edge i, j at layer l
F, D	Dimension of node and edge embeddings
$\mathcal{N}(i)$	All neighbors of node i
$\phi(\cdot)$	Differentiable message transformation function
$\mathcal{A}(\cdot)$	Permutation-invariant aggregation function
$\gamma(\cdot)$	Differentiable node transformation function

Table 3. Notations used in GNN definition.

where entries denote the out-degrees of each node. The second is the neighbor table, containing the row-major concatenation of the out-neighbors. Fig. 1 presents an example. Each consecutive slice (marked the same color) lists destination nodes coming from each source node. The third array (not shown) stores edge data. CSR format is beneficial when processing all edges with the same source node consecutively.

CSC. Compressed Sparse Column format is similar to CSR but using column-major order. In CSC format, the degree table stores the in-degree of each node, and the neighbor table is a column-major concatenation of the in-neighbors of each node. CSC format is beneficial when processing all edges with the same destination node consecutively.

Since the raw input graphs are in COO format, we develop an on-chip converter to transform into CSR or CSC as needed. The converter runs once when the graph is streamed into the FPGA and is reused for all the GNN layers.

3.3 Message Passing Mechanism

Most prevailing GNN architectures follow the message passing mechanism [18–23, 30–33]. With notation defined as in Table 3, the general computation of a message passing GNN can be expressed as:

$$x_i^{l+1} = \gamma(x_i^l, \mathcal{A}_{j \in \mathcal{N}(i)}(\phi(x_i^l, x_j, l, e_{i,j}^l)))$$

Fig. 2 demonstrates the message passing procedure for a single node n_1 at layer l , which will be repeatedly applied for all nodes and for several layers. Highlighted at the bottom of the figure, there are two major steps for each node in each layer of the GNN: *message passing (MP)* and *node embedding (NE)*. Message passing can be divided into “gather” and “scatter” phases, where “gather” corresponds to feature aggregation, and “scatter” corresponds to message transformation and passing. Node embedding involves node transformation and update.

Message Passing (Gather). In the “gather” phase, a.k.a., aggregation, of a certain node n_1 , the messages from its neighboring nodes obtained in the previous layer are retrieved from a message buffer. The messages are then aggregated in a permutation invariant manner, denoted by $\mathcal{A}(\cdot)$ (e.g., sum,

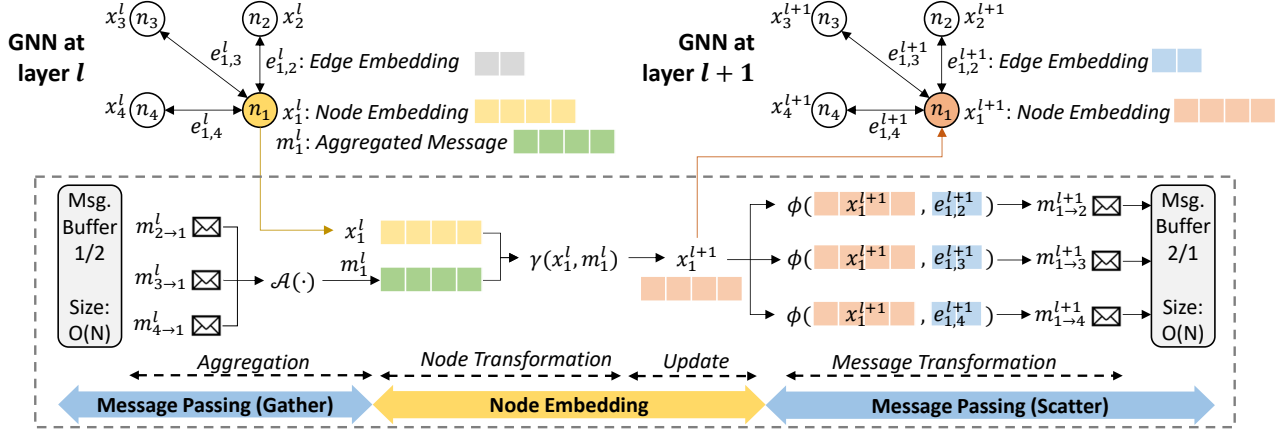


Figure 2. The generic message passing computation flow of prevailing GNN models.

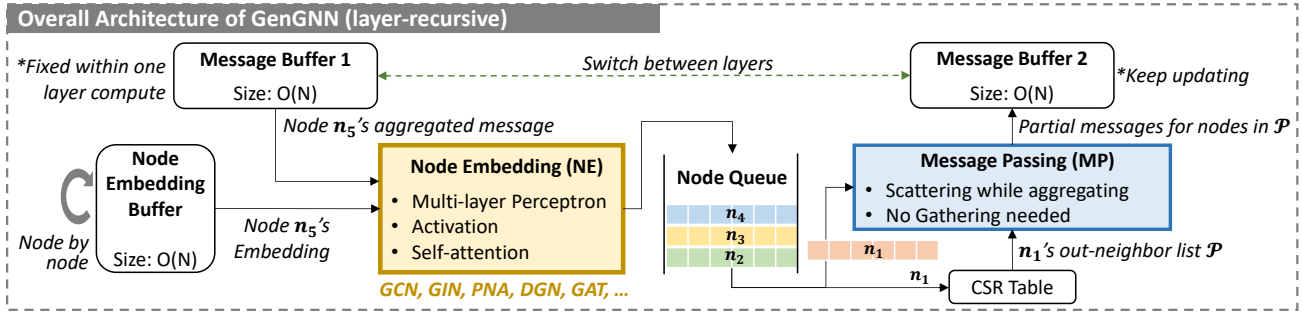


Figure 3. GenGNN overall architecture. It follows message passing mechanism and thus accommodates a wide range of GNNs.

max, mean, std. dev.). In advanced GNNs such as PNA, multiple aggregators are used with learnable weights and scaled according to the degree of the target node. The aggregated message is denoted by m_1^l .

Node Transformation. After aggregation, m_1^l is processed together with node n_1 's current node embedding, denoted by x_1^l , via a node embedding function, $\gamma(\cdot)$. $\gamma(\cdot)$ applies a node transformation using m_1^l and x_1^l , such as identity function, fully-connected layer, weighted sum of m_1^l and x_1^l , or an MLP applied to weighted sum or concatenation of m_1^l and x_1^l . After the transformation, $\gamma(\cdot)$ produces a new node embedding of n_1 , denoted by x_1^{l+1} , and applies the update.

Message Passing (Scatter). After node transformation is the "scatter" phase of message passing. The new node embedding x_1^{l+1} will be transformed by a message transformation function, $\phi(\cdot)$, usually together with an edge embedding $e_{src,dest}^{l+1}$, to generate the node's outgoing message. The message will be dispatched to all its neighbors, which will eventually be collected by the "gather" stage of the next layer.

A complete GNN model may consist of multiple layers, each with message passing and node embedding steps. For graph-level tasks, a global pooling layer is needed, possibly followed by MLP layers for final prediction.

3.4 High Level Hardware Framework

PEs and Buffers. We develop GenGNN following the message passing style. Fig. 3 illustrates the generic architecture. It has two main processing elements (PEs): node embedding (yellow block) and message passing (blue block), corresponding to the two steps described in Section 3.3. It has three data storage buffers: one node embedding buffer and two message buffers, all of size $O(N)$ where N is the number of nodes allowed on-chip. We temporarily assume that the whole graph can be stored on-chip and will discuss the extension to larger graphs that cannot fit in Section 4.6. The two message buffers act alternately across layers. For instance, message buffer 1 is read-only during layer 1 while message buffer 2 is being updated; during layer 2, message buffer 2 becomes read-only and buffer 1 updates.

Execution Flow. Fig. 3 illustrates the execution flow of one GNN layer. For multiple layers, the same resources and dataflow will be reused. Within one layer, the **node embedding PE** applies node transformation and update, e.g., MLP, activation, and self-attention. This is the main component that distinguishes different GNN models. Then, the **message passing PE** performs the subsequent scatter operation. Consider the graph in Fig. 2 as an example. Once node n_1 's embedding is updated, the MP PE retrieves its neighbors, i.e.,

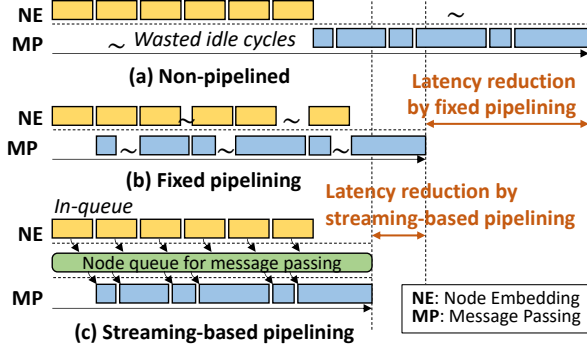


Figure 4. Different strategies of pipelining for node embedding and message passing.

n_2 , n_3 , and n_4 , computes the messages together with edge embeddings $e_{1,2}$, $e_{1,3}$, and $e_{1,4}$, and dispatches the messages. The receivers will instantly update their partially aggregated message in the message buffer. In this way, the scatter and gather phases can be merged, because the aggregation function is permutation invariant and the order of aggregation does not matter. Such a merged fashion has two merits. First, it reduces the overall process latency by fusing two stages into one. Second, it reduces memory cost from $O(E)$ to $O(N)$ where E is the number of edges and is typically much larger than N . This approach requires that the graph data is stored in its CSR format.

Note that an equivalent procedure is to first perform gather, i.e., aggregation, via incoming edges and then perform node transformation, in which case no scatter is needed. This approach requires two node embedding and one message buffer, all of size $O(N)$, and graph data stored in CSC format.

The NE and MP stages are connected by a FIFO (first-in first-out) queue, which enables pipelined execution. Details will be discussed in Section 3.5.

3.5 Node Embedding/Message Passing Pipeline

As demonstrated in Fig. 2, the two major steps, node embedding (NE) and message passing (MP), are dependent for a particular node but are independent across nodes and edges. This presents an opportunity to pipeline NE and MP to largely reduce processing latency.

Fig. 4 explains three strategies for NE and MP processing. **1 Non-pipelining.** In Fig. 4(a), NE and MP are not pipelined, which apparently suffers from a huge waste of idle cycles. **2 Fixed pipelining.** In Fig. 4(b), NE and MP are pipelined in a fixed manner: NE for the second node is pipelined with MP for the first node, etc. This achieves some latency reduction but suffers from imbalanced node degree. Specifically, if some nodes have larger degrees and their MP latency is longer than NE, while others have shorter MP latency, there still will be idle cycles. **3 Streaming-based pipelining.** In Fig. 4(c), NE and MP are pipelined flexibly

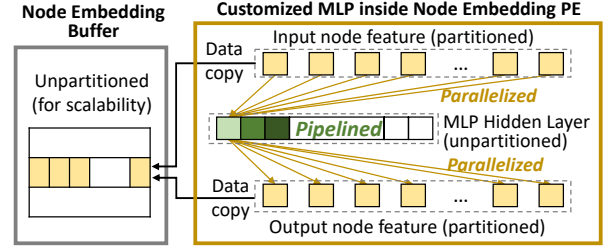


Figure 5. Customized MLP for GIN for node embedding.

using a node queue: as soon as a node finishes its NE, i.e., is ready for message passing, its embeddings are pushed into the queue; meanwhile, the MP engine will read from the queue and fetch the node embeddings for message passing. This scheme can be implemented using a streaming-based FIFO (first-in first-out) memory queue. This approach can greatly reduce the idle cycles and minimize the resource.

We acknowledge that our NE/MP pipeline shares a similar idea with the task scheduling in BoostGCN [13]. The differences are: 1) BoostGCN first sorts the vertices based on their degrees to determine an execution order on CPU, whereas we process on-the-fly in FPGA adaptively; 2) BoostGCN uses a buffer in external memory, whereas we build an on-chip FIFO to queue the nodes that are ready for message passing.

4 Model-Specific Components

4.1 Graph Isomorphism Network

GIN is representative of the GNN family whose message passing involves edge embeddings, and whose node transformation is computation intensive using MLPs. Each node's outgoing message is a weighted sum of its own node embedding and the outgoing edge embedding. Therefore, GIN adopts the CSR format converted from COO on-chip. Its message passing is within the framework using a customized message transformation function $\phi(x, m) = x^l + \epsilon^l \cdot m^l$.

For the computation-intensive MLP, we develop a customized MLP PE inside the node embedding PE, as shown in Fig. 5. For scalability and generality, the principle is *not* to apply optimizations to the node embedding and message buffers, but rather to allocate local buffers upon necessity. Therefore, the MLP PE has two local buffers fully-partitioned for inputs/outputs of one node, copied from/to the global node embedding buffer. Using ping-pong buffers, the data copy latency is overlapped with the MLP computation. We parallelize the multiplications at the partitioned input and output buffers and pipeline the execution along the MLP hidden layer elements. The designed MLP PE can be reused for other GNNs since MLP is a very common GNN operation.

4.2 Graph Attention Network

GAT is representative for its multi-head self-attention: each node’s incoming messages are first weighted before aggregation, where the attention coefficients are computed using the node and its neighbor’s embeddings. This exposes additional computation complexity, but fortunately, GAT is still fully compatible with GenGNN. Similar to GIN, GAT also needs a customized message transformation function, where $\phi(x, m) = x_i^l + \sigma_{i,j}^l \cdot m_j^l$, where $\sigma_{i,j}$ is the attention coefficient from node j to node i , computed using an attention function $\sigma_{i,j} = A(x_i, x_j)$ such as weighted sum or MLP.

The complexity of multi-head attention is proportional to the number of heads. Therefore, we parallelize along the head dimension in order to attain a speed-up while keeping the original node embedding and message buffers intact.

4.3 Principled Neighbor Aggregation

PNA uses multiple neighbor aggregations to increase the distinguishing power, where the node embedding is computed following [21]: $x_i^{l+1} = \text{relu}(\text{linear}(\bigoplus_{j \in \mathcal{N}(i)} (x_j^l)))$, and

$$\bigoplus = \left[\begin{array}{c} 1 \\ \log(D_i + 1)/\tilde{D} \\ \tilde{D}/\log(D_i + 1) \end{array} \right] \otimes \left[\begin{array}{c} \mu \\ \sigma \\ \max \\ \min \end{array} \right]$$

where D_i is the degree of x_i and $\tilde{D}$ is the average node degree seen in training data.

PNA falls into the message passing framework with a difference at the aggregation function. It has four aggregators including min, max, mean, and standard deviation; each aggregator stores its results into a separate buffer. All the scaling values are then computed and multiplied with the four aggregation values and written into a global buffer. Lastly, a pipelined linear-ReLU kernel is applied to compute the new node embedding, which reuses the MLP in the GIN model. Skip connections are added after each PNA layer computation to copy and accumulate embeddings from the output of the previous layer.

4.4 Directional Graph Networks

DGN [22] uses vector fields in a graph to define directional flows at each node that can be used for graph convolutions using anisotropic kernels. It uses eigenvectors of the graph Laplacian matrix to define directional aggregation matrices used in the “gather” phase of message passing.

Similar to its baseline PyTorch implementation, DGN accepts the precomputed Laplacian eigenvectors as a parameter and uses them to compute the relevant directional aggregation matrices on-the-fly during message passing. DGN uses two aggregations: the mean, and the directional derivative aggregation along the first eigenvector as $Y^l = \text{concat}\{D^{-1}AX^l, |B_{dx}^l X^l|\}$ where Y^l is the aggregated messages, the $X^{(l)}$ is the node embeddings, D is the degree matrix, A is the adjacency matrix, and B_{dx}^1 is the directional

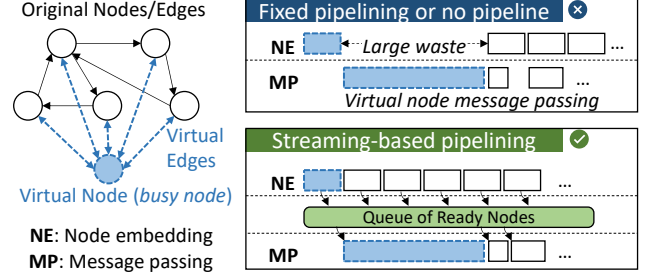


Figure 6. Streaming-based approach is especially beneficial for models with virtual nodes.

derivative matrix along first eigenvector. GenGNN is trivially extensible to other types of DGN aggregations, including directional smoothing B_{av} .

DGN’s node transformation uses an MLP with skip connections similar to PNA. The aggregation components run concurrently, as do the node transformations using each of the concatenated messages, enabling a total time complexity of $O(E + N)$ for each DGN layer.

4.5 Virtual Node

Our proposed streaming-based pipelining for node/edge processing (Section 3.5) is especially beneficial for models with virtual nodes. A virtual node [23] is an artificial node connected to all other nodes in the graph. The virtual node provides a shortcut for message passing between node pairs, which is demonstrated to be effective in many GNN models [34–36]. As illustrated in Fig. 6 left, a virtual node is *busy* with connections to all nodes, which results in highly unbalanced workload especially for large graphs and thus require special processing. In some models, there can be multiple virtual nodes [35] which escalates the model complexity.

Fortunately, benefiting from our proposed streaming-based pipelining for node/edge processing, the imbalance introduced by virtual nodes can be easily resolved without changing the framework. As shown in Fig. 6 right top, in fixed-pipeline or no-pipeline architectures, the process for the virtual node itself will take much longer time than others, resulting in a large waste. In contrast, as shown in Fig. 6 right bottom, in our proposed streaming-based architecture, processing of the virtual node can be fully overlapped with the node embedding computation for other nodes, with zero waste, as long as it is processed early enough (depending on the node ID numbering and processing order, which is adjustable). Effectiveness will be evaluated in Section 5.4.

4.6 Large Graph Extension

For large graphs that do not fit on-chip, our message passing mechanism is still applicable, i.e., the streaming-based pipeline working with two PEs, node embedding and message passing. However, additional strategic optimizations are necessary to hide memory access latency.

Model	DSP	LUT	FF	BRAM	URAM
Available	5,952	872K	1,743K	1344 (47 Mb)	640 (180 Mb)
GIN	817	66,326	81,144	365	10
GIN+VN	817	68,204	82,498	367	10
GCN	424	173,899	375,882	203	0
PNA*	50	40,951	34,533	233	144
GAT	341	80,545	82,829	484	0
DGN	1,042	73,735	93,579	523	0

Table 4. Resource utilization on Xilinx Alveo U50 FPGA. The clock frequency is 300 MHz. Results for the PNA* model are currently estimates from the Vitis HLS tool.

Prefetching. Synthesis of loop-carried dependences involving DRAM access can result in substantial overhead and is usually hard to pipeline. Since the graph is too big, its neighbor list stored in CSR format must be fetched from DRAM, which disrupts the pipeline inside message passing PE and introduces extra latency. To avoid this overhead, we develop a prefetcher, which fetches the degrees of consecutive nodes from DRAM into an on-chip FIFO buffer. The message passing PE loads each consecutive node’s degree as needed, triggering the prefetcher to refill the buffer. In this way, the latency of fetching from the off-chip degree table is completely hidden, and the message passing PE behaves in the same way as for small graphs.

Packed Data Transfers. For large graphs, the node embedding and message buffers are stored off-chip, while only the streaming FIFO and the prefetching results are stored on-chip. To alleviate the data transfer overhead and to saturate the AXI bus bandwidth, the off-chip data transfer must fully utilize the bus width. For example, transferring one 16-bit array element per clock cycle is a waste for a 64-bit bus. Therefore, we apply packed data transfer by typecasting off-chip array pointers to pointer types of a desired size, to transfer larger numbers of bits from and to DRAM each clock cycle. Given four 64-bit AXI buses, we pack 8 16-bit values and parallelize the fetching in one cycle, with an unpacking module reads 8 values in parallel. A similar technique is used to reduce DRAM writeback latency.

5 Experimental Results

5.1 FPGA Implementation

We implement **GenGNN** on Xilinx FPGA Alveo U50 accelerator card using Vitis HLS and Vivado. The available resources of U50 is shown in Table 4, and the FPGA logic runs at 300 MHz clock frequency. The graphs are streamed into the FPGA in their raw edge-list format (i.e., COO) consecutively with zero CPU intervention.

As listed in Table 2, we implement six GNN models, each being representative to a family of GNNs. Notably, each GNN model has a PyTorch version of implementation, to which we cross-check our on-board implementation and guarantee

Dataset	Nodes	Edges	Feat. Dim.	LUT	FF
Cora	2,708	10,556	1,433	111,456	110,508
CiteSeer	3,327	9,104	3,703	116,442	109,765
PubMed	19,717	88,648	500	119,329	100,699

Table 5. The three datasets used to test DGN with Large Graph Extension, along with their corresponding resource utilization. GenGNN with the Large Graph Extension utilizes 1,344 DSPs, 494 BRAMs, and 0 URAMs for all three datasets.

that our end-to-end execution is correct. For GCN, GIN, and GIN-VN, the number of layers is 5 and the node embedding dimension is 100, as specified in the PyTorch model [37]. All of these models also use global average pooling, and an output head with a single linear layer. For PNA, we use 4 layers with an node embedding dimension of 80, global average pooling, and an MLP-ReLU head with sizes (40, 20, 1). For DGN, we use 4 layers and a node embedding dimension of 100, global average pooling, and an MLP-ReLU head with sizes (50, 25, 1). For GAT, we use 5 layers with 4 heads and 16 features per layer, global average pooling, and an output head with a single linear layer. The resource utilization of all models are reported in Table 4, and the resource utilization for Large Graph Extension is reported in Table 5.

We also would like to point out that we do not over-optimize the code, since this work is to demonstrate the architectural advantages of our framework. We deliberately omit some optimizations, for example, conservatively using 32-bit fixed point quantization (Large Graph Extension uses 16-bit); we also do not make optimizations over the parameters that may be unscalable (e.g., partitioning the dimension of maximum number of nodes).

The FPGA latency is measured *end-to-end on-board*, obtained from the “average execution time” in the OpenCL summary report after the execution of all testing graphs.

5.2 Dataset and Baseline

Datasets. We use three datasets to evaluate **GenGNN**. For real-time processing evaluation, we adopt two molecular property prediction datasets, MolHIV and MolPCBA, from the Open Graph Benchmark [38]. Both are *graph-level* tasks. MolHIV testing set has 4k graphs and MolPCBA testing set has 43k graphs. For large-scale extension evaluation, we adopt three prevailing classification datasets, CiteSeer, Cora [39], and PubMed [40], where the graphs are much larger and cannot fit into on-chip memory. All three are *node-level* tasks.

Baseline. We take CPU (Intel Xeon Gold 6226R) and GPU (NVIDIA RTX A6000) executions as the baseline. We average five iterations of the time measured on CPU and GPU, where each model is implemented in PyTorch Geometric [41] with identical hyperparameters to their corresponding accelerator with batch size of 1. Although we would like to

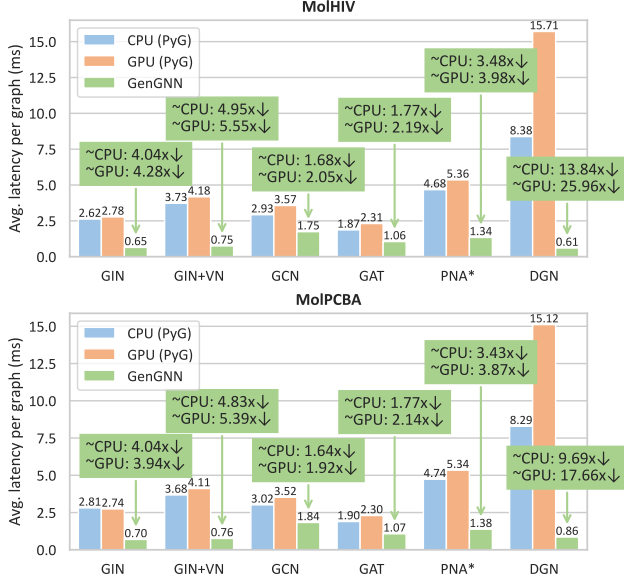


Figure 7. Average latency over test graphs. Top shows MolHIV results; bottom shows MolPCBA results. Results for the PNA* model are currently estimates from the Vitis HLS tool.

compare with existing FPGA accelerators [9, 13], we cannot find the GNN details such as the number of layers and node embedding dimensions, and they only provide GCN results. More importantly, since we target real-time applications, we do not employ any preprocessing for the input graphs, while both [9] and [13] perform graph partitioning and [13] conducts graph-specific optimizations. Therefore we find it difficult to make a fair comparison.

5.3 End-to-end Evaluation

We fully evaluate GenGNN using six GNN models by comparing with CPU and GPU baselines. The results are depicted in Fig. 7. The top figure uses the MolHIV dataset and the bottom figure uses the MolPCBA dataset. It shows that for six GNN models, on MolHIV, GenGNN achieves 1.77–13.84× speed-up compared with CPU, and 2.05–25.96× speed-up compared with GPU; on MolPCBA, GenGNN achieves 1.64–9.69× speed-up compared with CPU, and 1.92–17.66× speed-up compared with GPU. It invariably demonstrates the effectiveness of GenGNN, especially given that we do not over-optimize our models but only exhibit the advantages of the framework itself. Meanwhile, the most prominent speed-up is the DGN model (up to 25.9×), presumably because CPU and GPU are not specialized for the directional derivative aggregation (Section 4.4), which implies the necessity of customized FPGA accelerating components.

Next we evaluate the scalability of GenGNN to support large graphs that do not fit on-chip. Table 5 summarizes the graph size and node feature dimension (Feat. Dim.) for each benchmark. Fig. 8 depicts the comparisons with CPU and

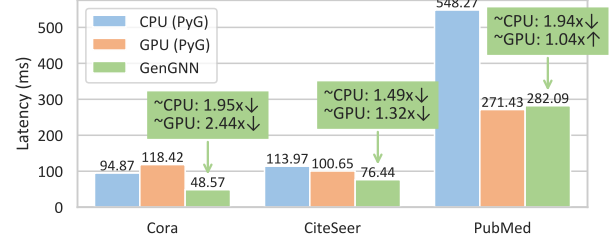


Figure 8. Latency of GenGNN DGN with Large Graph Extension over Cora, CiteSeer, and PubMed graphs.

GPU. Compared with CPU, GenGNN achieves 1.49–1.95× speed-up; compared with GPU, it is 2.44× faster on Cora, 1.32× faster on CiteSeer, but 1.04× slower on PubMed. Since the main focus of this work is not on large graphs, we will improve in future works.

5.4 Streaming-based Pipelining Evaluation

Fig. 9 demonstrates the effectiveness of the proposed streaming-based pipelining (Section 3.5) on both synthetic graphs and real benchmarks using the GIN model implementation. First, we test 100k random graphs with various statistics in Fig. 9(a), including average node degree (x-axis) and the percentage of large-degree nodes (y-axis). The x-axis is grouped every three columns by the same average node degree. Within each group, the first column is the speed-up of fixed-pipeline over non-pipeline (1.2~1.5×); the second is the speed-up of streaming-based over fixed-pipeline (1.15~1.37×); and the third is streaming-based over non-pipeline (1.53~1.92×).

A general trend can be observed that when the average node degree is smaller and there are fewer high-degree nodes, the streaming pipeline is more beneficial. The reason is that the more imbalanced the latency of node embedding and message passing, the more beneficial streaming becomes in utilizing both PEs. When the node degree is large and the message passing dominates the latency (i.e., the node embedding latency is mostly shorter than the message passing), the streaming-based pipeline will degrade to fixed-pipeline.

We also verify its effectiveness on real benchmarks from the MolHIV dataset as well as with virtual nodes. Fig. 9(b) shows the speed-up of fixed and streaming pipelines, 1.38× and 1.63×, respectively; Fig. 9(c) shows the speed-up with virtual nodes, 1.40× and 1.61×, respectively. This implies that the streaming-based pipeline is efficient in reducing processing latency. It also reduces memory cost since we set the queue depth to be 10 nodes.

6 Conclusion

In this work, we proposed **GenGNN**, the first generic and flexible FPGA accelerator framework for a wide range of GNNs. Its noteworthy features include generality for future-proofing, real-time processing, and open-source. GenGNN is

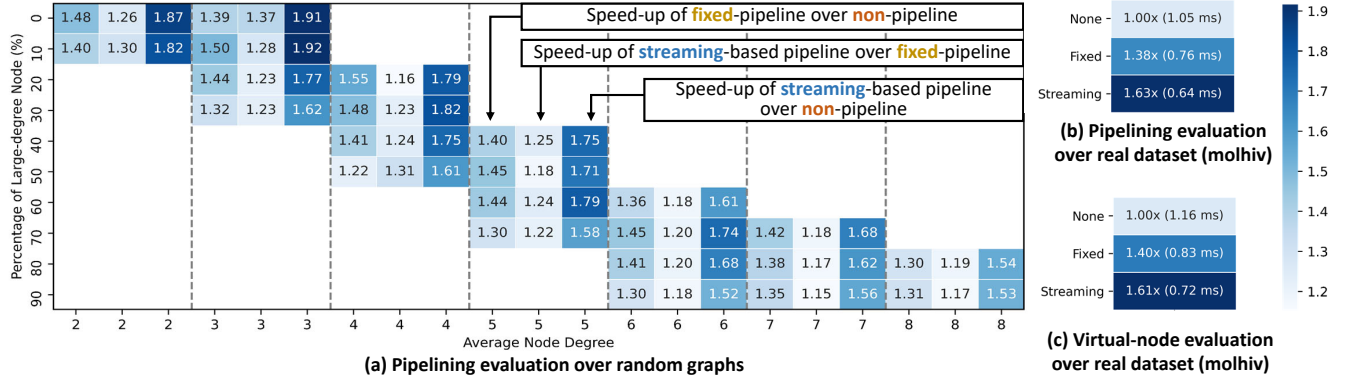


Figure 9. Speed-up of NE/MP pipelining techniques: fixed- and streaming-based pipeline over non-pipeline. Fixed-pipeline is up to 1.5 $\times$ faster than non-pipeline; streaming-based is up to 1.37 $\times$ faster than fixed and 1.92 $\times$ faster than non-pipeline.

composed of an optimized message-passing structure applicable to all models, combined with a rich library of model-specific components. On-board evaluation with guaranteed functionality exhibited invariant speed-up comparing with CPU and GPU baselines, as well as the effectiveness of our streaming-based pipeline architecture within message passing mechanism. We also demonstrated its scalability by extending to commonly used large graphs with speed-up. Future work includes design automation, design space exploration, and large graph optimization for GenGNN.

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